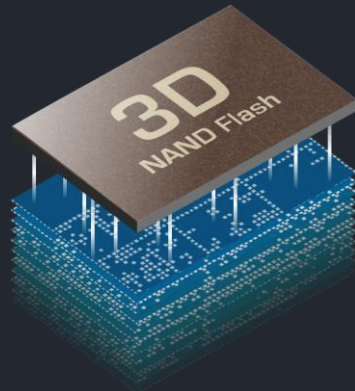


# JTS250F HIGH-SPEED NAND TESTER

Product Brief

Access at anytime with our small, convenient and fast testing tools.



Sep.2019



# Features & Advantages

## Software-defined Pattern Generator

- Software-defined pattern generation logic provides very flexible and easy test programming environment for test engineer.

## FPGA-based Timing Generator

- SDR mode: support legacy mode
- DDR mode: support source synchronous ddr mode clocking

## Programmable Voltage & Frequency

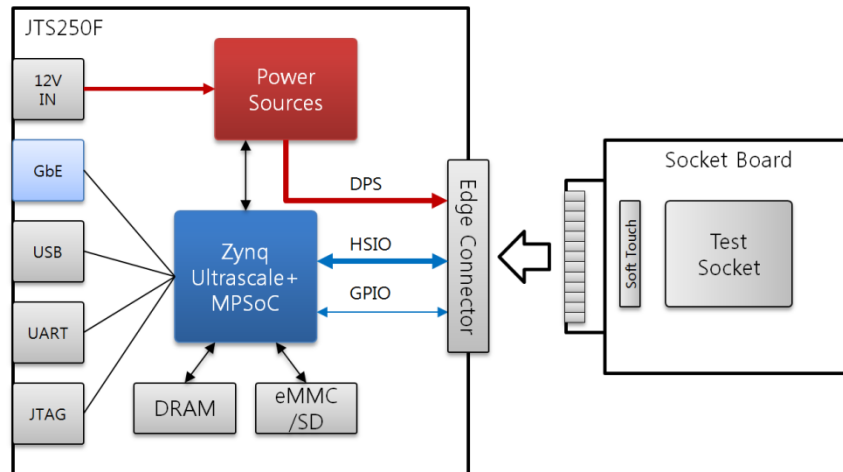
- Programmable power supplies (VCC, VCCQ, VPP, VCCIO, VREF, VREFIO)
- Programmable test speed up to 800 MHz

## Best Signal Integrity

- Best signal integrity for high speed I/Os (HSIO)
- Additional general purpose I/Os (GPIO)

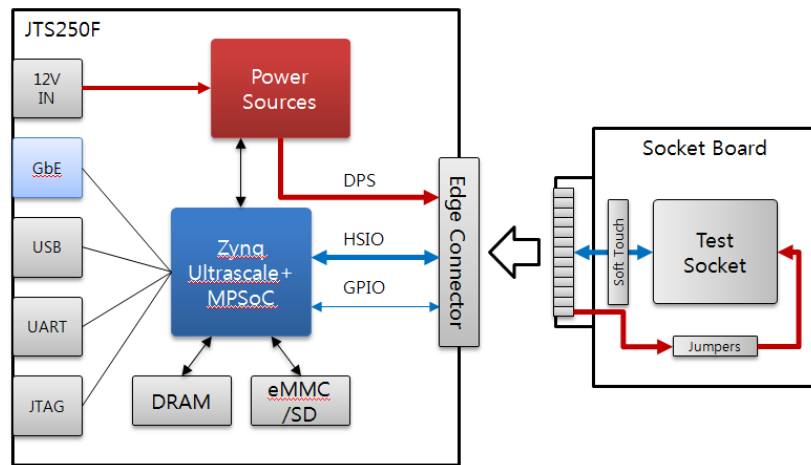
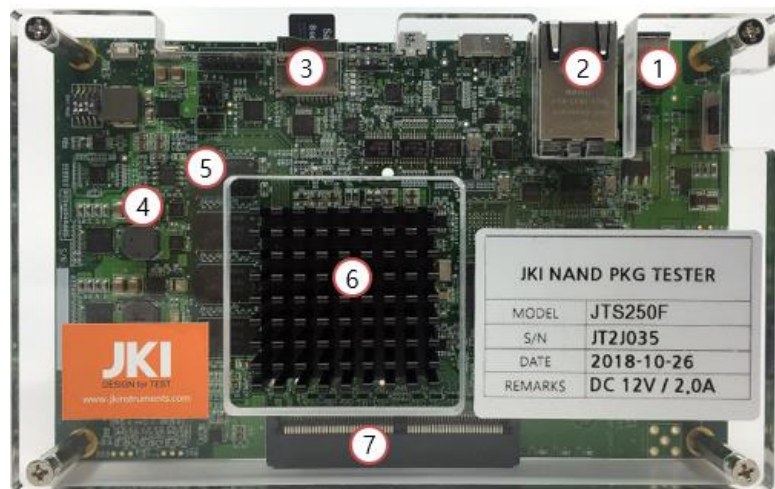
## Applications

- Engineering test solution for high-speed DDR NAND devices



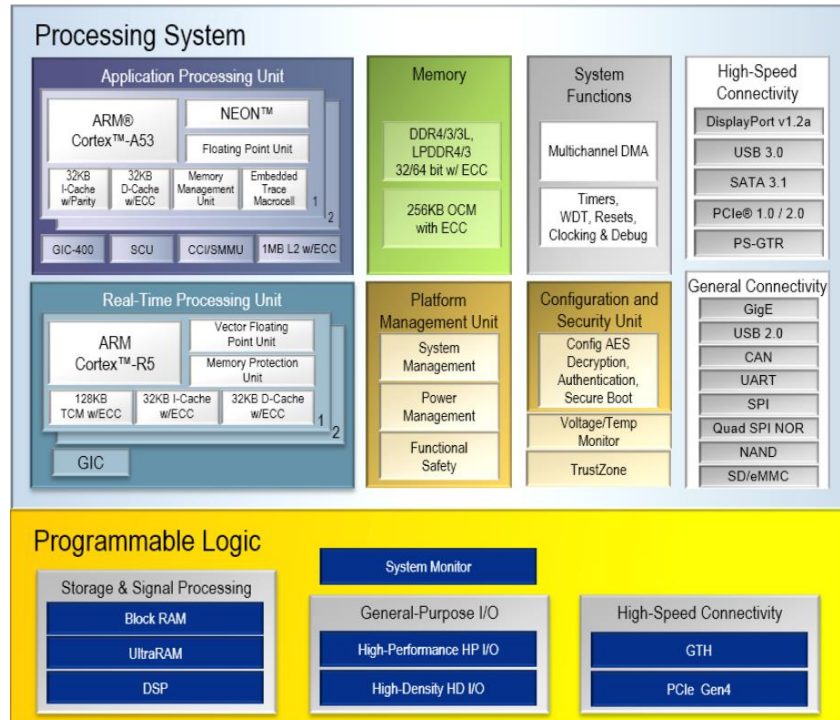
# Test Board

- ① Main Power Supply: 12V DC input
- ② Host Interface: Gigabit Ethernet
- ③ SD Card: Booting image and Firmware
- ④ Programmable Device Power Supplies
- ⑤ DRAM: Application Memory
- ⑥ Zynq (MPSoC + FPGA): Pattern Sequencer and Generator
- ⑦ Edge connector to connect Test board and Socket board

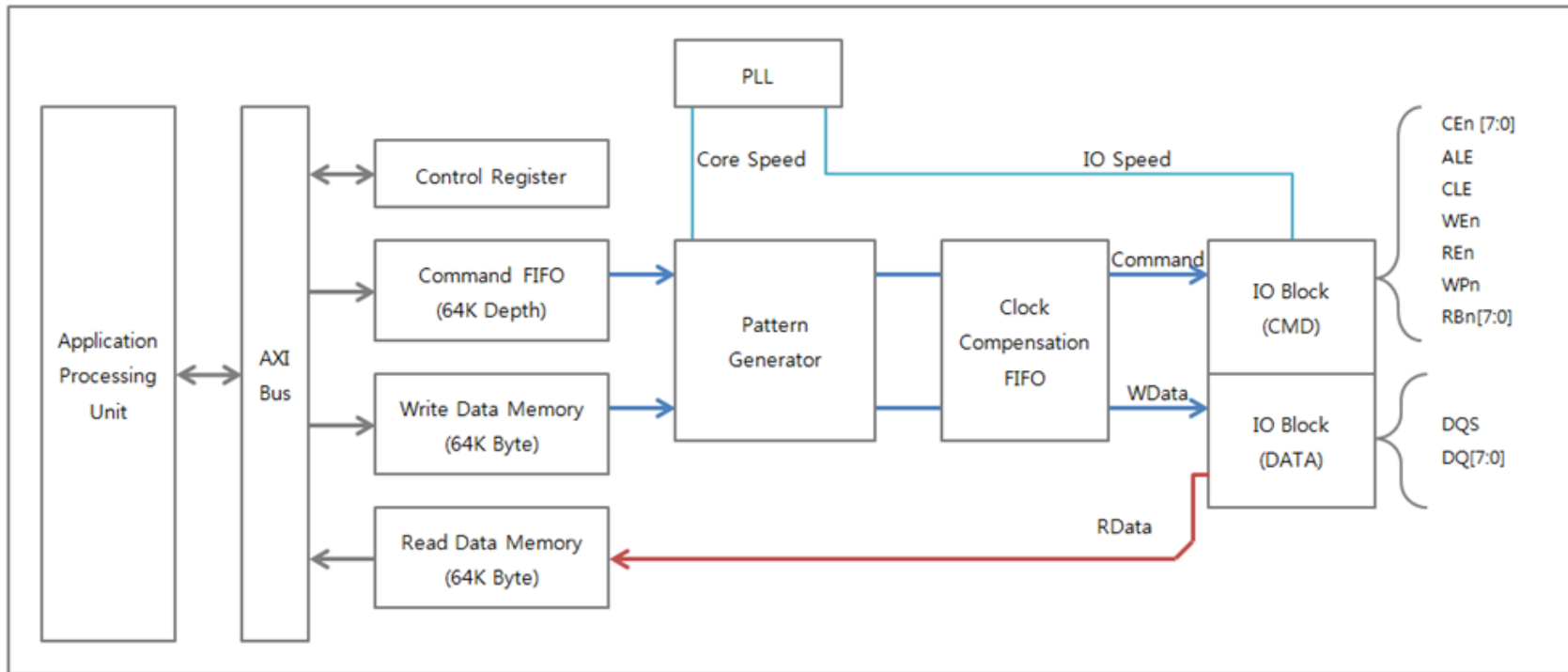


# Pattern Controller

Pattern Controller Specification		
<b>Processor</b>	Application Processor	Dual-core ARM Cortex-A53
	Real-time Processor	Dual-core ARM Cortex-R5
<b>Memory</b>	Application Memory (DRAM)	2GB
	Micro-SD	8GB
	eMMC	8GB
<b>Peripheral</b>	Ethernet	1G Ethernet
	USB	USB2.0
<b>Debug</b>	UART(USB)	USB to UART Bridge
	JTAG	14pin/2.0mm



# Pattern Generator



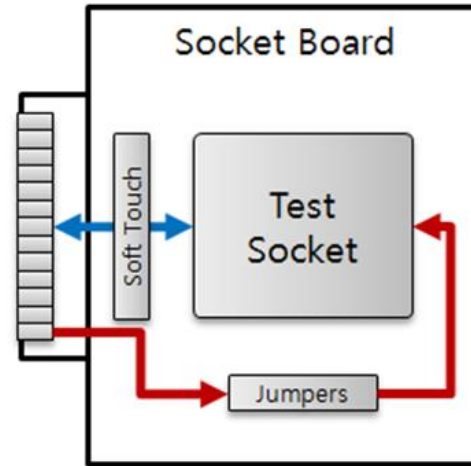
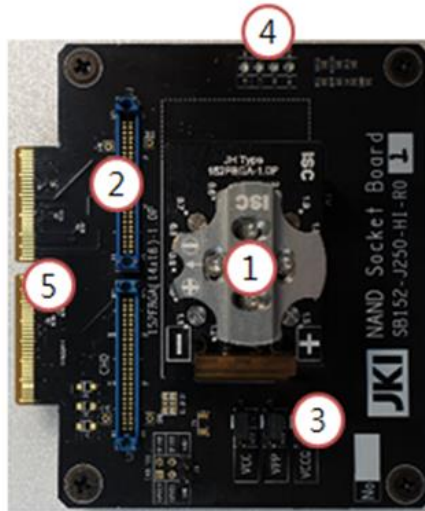
# Device Power Supply

1. VCC: NAND device core power supply.
2. VCCQ: NAND I/O power supply.
3. VPP: NAND external high voltage.
4. VREF: NAND I/O reference voltage.
5. VCCIO: FPGA I/O power supply.
6. VREFIO: FPGA I/O reference voltage

Device Power Supply Specification				
Power Sources	Setting Range	Resolution	DC Accuracy	Max. Current
VCC (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	1.2A
VCCQ (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	400mA
VPP (NAND)	5.0 to 20V	50mV	+/- (2% + 100mV)	80mA
VREF (NAND)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA
VCCIO (FPGA)	0.8 to 2.0V	1mV	+/- (1% + 20mV)	400mA
VREFIO (FPGA)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA

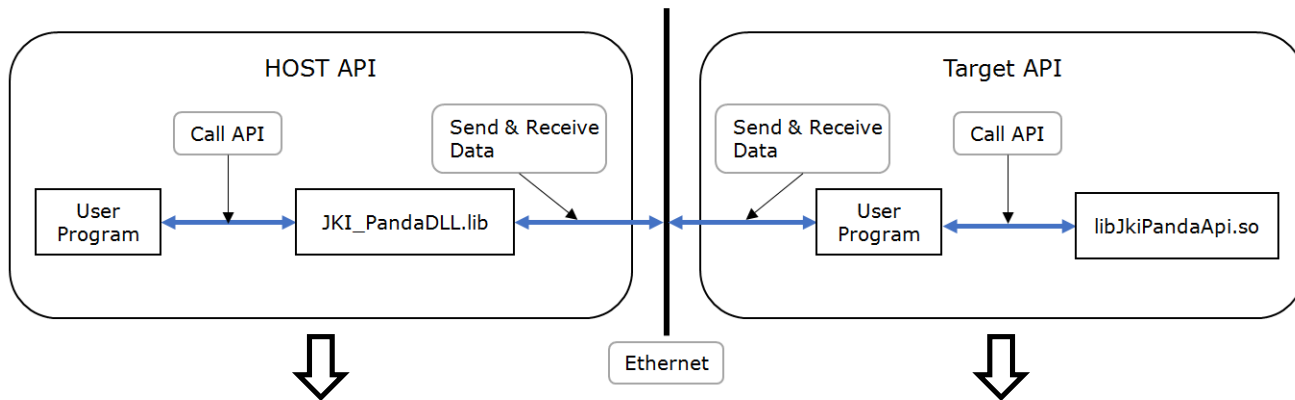
# Socket Board

- ① Test Socket
- ② Logic analyzer probing pad
- ③ Power jumpers
- ④ LED indicators
- ⑤ Edge card





# Software Architecture



Running on Remote PC (Host)

Running on Zynq Processor (Target)

CH	CE	DIO#	3000	158	4.80	2387	2425	2427	2500	3132	3569	3485	3114
CH	CE	DIO#	3000	158	4.80	2387	2425	2427	2500	3132	3569	3485	3114
CH	CE	DIO#	3000	158	4.80	2387	2425	2427	2500	3132	3569	3485	3114
CH	CE	DIO#	3000	158	4.80	2387	2425	2427	2500	3132	3569	3485	3114

```

[2019-02-15 14:18:27] DistributionWithSLC Complete!!
[2019-02-15 14:17:06] <TLC MODE> NAND Reset Start!! [Channel:01 CE:01 Dio:00]
RESET = Bus
[2019-02-15 14:17:06] NAND Reset Complete!!
[2019-02-15 14:17:06] <TLC MODE> Read ID Start!! [Channel:01 CE:01 Dio:00]
===== READ ID =====
jst 2nd 3rd 4th 5th 6th 7th 8th
CH C1 DIO# FF FF FF FF FF FF FF
===== UNIQUE ID =====
UNIQUE ID : A0 00 29 05 2F 15 00 31
-----
[2019-02-15 14:17:06] Read ID Complete!!
[2019-02-15 14:17:06] <TLC MODE> Erase Start!! [Channel:01 CE:01 Dio:00]
CH CE LUN STATE Blk P/F 26845 MAIN PBL50C
CH C1 LUN0 ERASE_PLANE_TLC 300 PASS 4609 256 255
[2019-02-15 14:17:06] Erase Complete!!
[2019-02-15 14:17:06] <TLC MODE> Program Start!! [Channel:01 CE:01 Dio:00]
CH CE LUN State BLOCK ML STRING L58 C58 M58 P/F
CH C1 LUN0 PGR_PLANE_TLC 300 ML000 STR2160 000 001 002 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML000 STR2160 000 004 005 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML000 STR2162 000 007 008 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML000 STR2163 000 010 011 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML001 STR2168 012 013 014 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML001 STR2163 015 016 017 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML001 STR2160 018 019 020 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML001 STR2163 021 022 023 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML002 STR2160 024 025 026 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML002 STR2163 027 028 029 FAIL
CH C1 LUN0 PGR_PLANE_TLC 300 ML002 STR2163 030 031 032 FAIL
    
```

```

./main -r -t
1970-01-01 03:55:03 [INFO] JKI Panda API 1.4.6.a (20190422) - Copyright (c) 2018 JKI Inc.
1970-01-01 03:55:03 [INFO] PandaHal
[IntBoard]
HwVersion = 0x00000400
FwVersion = 0x20190422
RomVersion = 0x00004500
[NandSetTarget] DEVICE TYPE = SOCKET TYPE_152B_RAM_HS, Channel = 0
RunNandSampleTest: , Mode = 1, freq: 400.000, ce: 0
[SetClock] set: 400.000 MHz, get: 400.004 MHz
1970-01-01 03:55:04 [INFO] NandSetMode> mode: 0 (SDR)
[NandReset] Busy = 0.300 us
[NandReadId] Add = 00, Data = ad-7e-28-33-00-a0- (0 / gbytes)
[NandReadId] Add = 40, Data = 4a-45-44-45-43-02- (6 / gbytes)
[NandSetFeature] Add = 02, Data = 37-00-33-00-, Busy = 0.490 us
[NandSetFeature] Add = 02, Data = 37-00-33-00- (4 / 4 bytes), Busy = 0.490 us
[NandSetFeature] Add = 01, Data = 60-00-01-00-, Busy = 0.490 us
1970-01-01 03:55:04 [INFO] NandSetMode> mode: 1 (DDR)
[NandGetFeature] Add = 01, Data = 60-60-00-00-01-01-00-00- (8 / 8 bytes), Busy = 0.490 us
[NandEraseSic] Busy = 4002.610 us
[NandProgramSic] CE = 0, Row = 100, Col = 0, Busy = 110.740 us
Data (9216 bytes) = 67-c6-69-73-51-ff-4a-ec-29-cd-ba-ab-f2-fb-e3-46-
[NandPageReadSic] CE = 0, Row = 100, Col = 0, Busy = 44.900 us
Data = 67-c6-69-73-51-ff-4a-ec-29-cd-ba-ab-f2-fb-e3-46- (9216/9216 bytes)
=====
! -> Pass
=====
1970-01-01 03:55:04 [INFO] ~PandaHal
    
```

# Product Specifications

## Pattern Controller Specification

<b>Processor</b>	Application Processor	Dual-core ARM Cortex-A53
	Real-time Processor	Dual-core ARM Cortex-R5
<b>Memory</b>	Application Memory (DRAM)	2GB
	Micro-SD	8GB
	eMMC	8GB
<b>Peripheral</b>	Ethernet	1G Ethernet
	USB	USB2.0
<b>Debug</b>	UART(USB)	USB to UART Bridge
	JTAG	14pin/2.0mm

## Pattern Generator Specification

<b>Pattern Generator</b>	Command FIFO depth	64K
	Write Data Memory	64K Byte
	Read Data Memory	64K Byte
<b>Clock Generator</b>	Speed (SDR mode)	10 MHz
	Speed (DDR mode)	200 MHz ~ 800 MHz
	Resolution	< 1 MHz
<b>Channels</b>	Output (CEn[7:0], ALE, CLE, WEn, RE, WPn)	22 pins * 2-channel
	Input (RBn[7:0])	8 pins * 2-channel
	I/O (DQS, DQ[7:0])	10 pins * 2-channel
	GPIO	8 pins

## Device Power Supply Specification

Power Sources	Setting Range	Resolution	DC Accuracy	Max. Current
VCC (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	1.2A
VCCQ (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	400mA
VPP (NAND)	5.0 to 20V	50mV	+/- (2% + 100mV)	80mA
VREF (NAND)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA
VCCIO (FPGA)	0.8 to 2.0V	1mV	+/- (1% + 20mV)	400mA
VREFIO (FPGA)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA

## Environment Conditions

<b>Operating Temperature</b>	0 ~ 70 °C
<b>Humidity</b>	20% ~ 60 Rh%
<b>Dimensions &amp; Weight</b>	160 mm x 100 mm x 38mm ( W x L x H )
<b>Power Supply</b>	DC 12V / 2A
<b>Host Interface</b>	Ethernet

■ *trace*

▲ *test*

● *verify*

+ *connect*