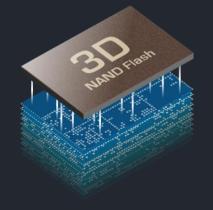
# JTS250F HIGH-SPEED NAND TESTER

**Product Brief** 

Access at anytime with our small, convenient and fast testing tools.





Sep.2019

# Solution Brief

Connect	Test	Тгасе	Verify
<ul> <li>Connect Solution</li> <li>High-speed socket board</li> <li>Burn-in socket board</li> <li>Best signal quality and impedance matching</li> <li>Logic probing pad</li> </ul>	<ul> <li>Test Solution</li> <li>Software-defined pattern</li> <li>Hardware-based timing</li> <li>Programmable Voltage &amp; Frequency</li> <li>Embedded Linux and host programming environments</li> </ul>	Trace Solution • Trace and debug with JKI NAND protocol analyzer • Wave view • List view • Packet decoding	Analysis Solution • NAND protocol analysis • NAND cell analysis • Power & Speed margin test • User test APIs
	<pre>static void NandPageRead(byte ch, byte ce, in nand.SelectCE(ce); nand.Command(0xA2); // SLC mode transition nand.Command(0x00); // 1st set nand.AddressCol(col); // Address cycle nand.AddressRow(row); // Address cycle nand.CmdWithBusy(0x30, ce); // 2nd set: t nand.ReadBytes(ref data, length); // Read nand.DeselectCE(ce); }</pre>	on ER (70us / 80us)	AndExes         Ci: 0, Ci: 0, DOI: 000000000           [10]         Weitheweiticz, weither 1:0:0:0           [10]         Weitheweiticz,
V V V V V V V V V V V V V V V V V V V			<ul> <li>(AC) = 1 separatinew - 74,230 m</li> <li>(AC) = 1 separatinew - 74,230 m</li> <li>(BC) = 1 separatinew - 74,200 m</li> <li>(BC) = 1 separatinew - 74,000 m</li> <li>(BC) = 1 separatinew - 74,0</li></ul>
2020-02-19	JKI Col	nfidential	

## Features & Advantages

### Software-defined Pattern Generator

 Software-defined pattern generation logic provides very flexible and easy test programming environment for test engineer.

### FPGA-based Timing Generator

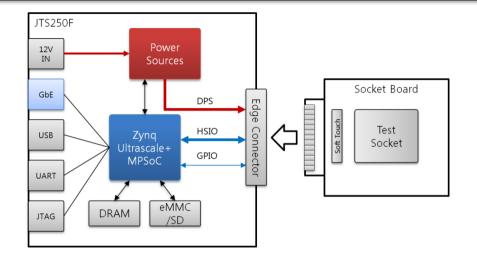
- SDR mode: support legacy mode
- DDR mode: support source synchronous ddr mode clocking

### Programmable Voltage & Frequency

- Programmable power supplies (VCC, VCCQ, VPP, VCCIO, VREF, VREFIO)
- Programmable test speed up to 800 MHz
- Best Signal Integrity
  - Best signal integrity for high speed I/Os (HSIO)
  - Additional general purpose I/Os (GPIO)

Applications

 Engineering test solution for high-speed DDR NAND devices



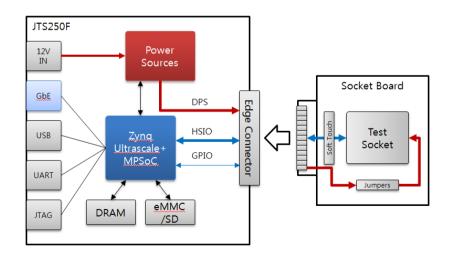


#### JKI Confidential

## Test Board

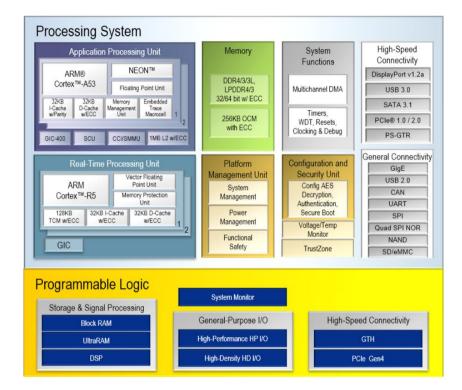
- ① Main Power Supply: 12V DC input
- ② Host Interface: Gigabit Ethernet
- ③ SD Card: Booting image and Firmware
- ④ Programmable Device Power Supplies
- 5 DRAM: Application Memory
- 6 Zynq (MPSoC + FPGA): Pattern Sequencer and Generator
- ⑦ Edge connector to connect Test board and Socket board



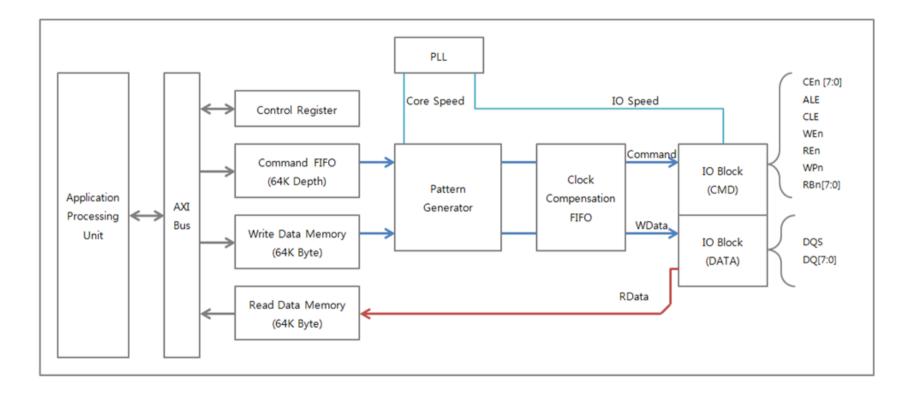


## Pattern Controller

Pattern Controller Specification					
Processor	Application Processor Dual-core ARM Cortex-A53				
	Real-time Processor	Dual-core ARM Cortex-R5			
Memory	Application Memory (DRAM)	2GB			
	Micro-SD	8GB			
	eMMC	8GB			
Peripheral	Ethernet	1G Ethernet			
	USB	USB2.0			
Debug	UART(USB)	USB to UART Bridge			
	JTAG	14pin/2.0mm			



## Pattern Generator



# **Device Power Supply**

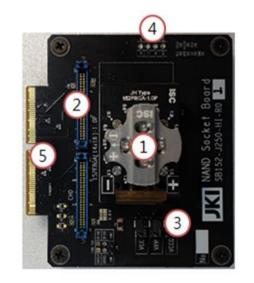
- 1. VCC: NAND device core power supply.
- 2. VCCQ: NAND I/O power supply.
- 3. VPP: NAND external high voltage.
- 4. VREF: NAND I/O reference voltage.
- 5. VCCIO: FPGA I/O power supply.
- 6. VREFIO: FPGA I/O reference voltage

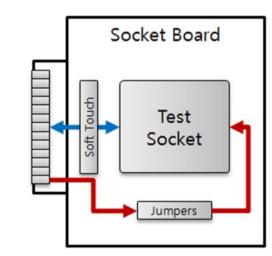
## **Device Power Supply Specification**

Power Sources	Setting Range	Resolution	DC Accuracy	Max. Current
VCC (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	1.2A
VCCQ (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	400mA
VPP (NAND)	5.0 to 20V	50mV	+/- (2% + 100mV)	80mA
VREF (NAND)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA
VCCIO (FPGA)	0.8 to 2.0V	1mV	+/- (1% + 20mV)	400mA
VREFIO (FPGA)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA

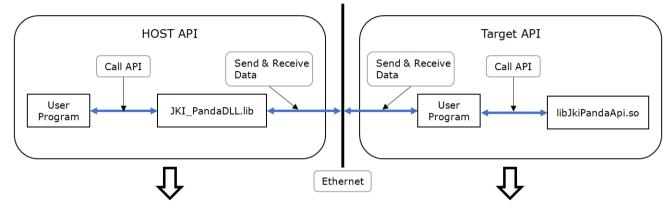
# Socket Board

- 1 Test Socket
- ② Logic analyzer probing pad
- ③ Power jumpers
- ④ LED indicators
- 5 Edge card





## Software Architecture



#### Running on Remote PC (Host)

System Info			PGM SEQUENCE		011	CEO	DIED	300	158	4.80	2387	2425	2427	2500	3132	3569	3485	3114
S W:201	81220	INIT	V NAND Reset		CH1	CEO	DIEG	300	150	4.90	3784	3632	3695	3617	3894	2754	2945	3247
H W:000 FPGA:000		DIAG	2 Read ID		CH1	CEO	DIE8 14:16:2	300	162	5.00		12160	12079	11698	12226	12209	11965	1203
FPGA : 000	04300	Multi Board Test	NAND Para Reset		1201		1411014	1 0120	- IDUCI	onations	cc comp.	erent						
		1 .	Show All Parameters				14:17:0	6] «TLO	MODE>	NAND R	eset Sti	rtll [0	Channel:	:01 CE:	01 Die:	10]		
		NAND Type	NAND Select DDR			• Ous	14:17:0				a an an							
Power Info		\$72_TLC_256Gb +	NAND GetFeature		[201	+02+15	14:17:0	ioj revito	Reset	comple	tell							
Conter Bille		Controller	C Erase				14:17:0											
		NONE -	Program				10								8th			
		Operation Mode	Read		CH1	CE1	DIE0	FF 1st	FF 2nd	FF 3rd	FF 4th	FF	FF 6th	FF 7th	FF			
		TLC +	DistributionWithSLC			E IO :	10.000	AD	08	29	85	28	15	00	31			
Log I	Deplay	#ofCH #ofCE #ofLUN	Read Vths of Cells															
ON +	ON .	2C • 2C • 1L •	TestGpioCtrl															
OH# CE#	LUNA	TEST START	E3 recopiocol		1201	-02-15	14:17:0	61 Read	1 ID Cor	moletel								
1 1	0	TEST STOP																
StartBLK	LastBLK	and the second se			[2019 CH	-02-15 CE	14:17:0	STATE		Erase		[Channe P/F						
	300	Clear Screen			OI	CE1	LUN		1PLANE	TLC	8LK 300	P/F PASS		256	PHL500 255			
StartPape	LastPage	Add to List			[201		14:17:0											
	16	Remove from List					14:17:0							-				
ReadStep	PagaStep	Links and the second			CH [ 261	CE	14:17:0	State		Progra	BLOCK		STRING		LSB	CSB	MSB	
5	1	Remove All			CH1	CEI	LUNG	PGM_1	PLANE_T		300		STRING		000	001	002	FAIL
Option1	Option2	TEST START Listed	×	ð	CH1		LUNO		PLANE_T		300	ML000	STRING		003	004	005	FAIL
1	0	NONE -	Function Tip	Listed Function Tip	CH1 CH1	CEI	LUND		PLANE_T		300 300	ML000			005 009	007 010	008 011	FAIL FAIL
-			Save List	Load List	011	CEI	LUNO		PLANE T		300	HL000	STRING		012	013	014	FAIL
	-	8	Jarre Los	LOBULOC	CH1	CE1	LUNO	PGH_1	PLANE_T		300	<b>HL001</b>	STRING		015	016		FAIL
					CH1		LUNB		PLANE_1		300	<b>WL001</b>	STRING			019	020	FAIL
					CH1 CH1	CE1	LUNO		PLANE_T		300 300	16.001	STRING		021 024	022	023 026	FAIL
					011	CE1 CE1	LUNA		PLANE_T		300	ML002			024 027	025 028	026 029	FAIL
					OH	CEI	LUNA		PLANE_I		100		STRING		010	011	832	FATL

#### **Running on Zynq Processor (Target)**

zyng> ./main -r -t
1970-01-01 03:55:03 [INFO] JKI Panda API 1.4.6.a (20190422) - Copyright (C) 2018 JKI Inc.
1970-01-01 03:55:03 [INFO] PandaHal
[InitBoard]
HwVersion = 0x00000400
FwVersion = 0x20190422
RomVersion = 0x00004500
[NandSetTarget] DEVICE_TYPE = SOCKET_TYPE_152B_RAW_HS, Channel = 0
RunNandSampleTest: , mode: 1, freq: 400.000, ce: 0
[SetClock] set: 400.000 MHz, get: 400.004 MHz
1970-01-01 03:55:04 [INFO] NandSetMode> mode: 0 (SDR)
[NandReset] Busy = 0.300 us
[NandReadId] Add = 00, Data = ad-7e-28-33-00-a0- (6 / 6bytes)
[NandReadId] Add = 40, Data = 4a-45-44-45-43-02- (6 / 6bytes)
[NandSetFeature] Add = 02, Data = 37-00-33-00-, Busy = 0.490 us
[NandGetFeature] Add = 02, Data = 37-00-33-00- (4 / 4 bytes), Busy = 0.490 us
[NandSetFeature] Add = 01, Data = 60-00-01-00-, Busy = 0.490 us
1970-01-01 03:55:04 [INFO] NandSetMode> mode: 1 (DDR)
[NandGetFeature] Add = 01, Data = 60-60-00-01-01-00-00- (8 / 8 bytes), Busy = 0.490 us
[NandEraseSlc] Busy = 4002.610 us
[NandProgramSlc] CE = 0, Row = 100, Col = 0, Busy = 110.740 us
Data (9216 bytes) = 67-c6-69-73-51-ff-4a-ec-29-cd-ba-ab-f2-fb-e3-46-
[NandPageReadSlc] CE = 0, Row = 100, Col = 0, Busy = 44.900 us
Data = 67-c6-69-73-51-ff-4a-ec-29-cd-ba-ab-f2-fb-e3-46- (9216/9216 bytes)
1 -> Pass
1970-01_01 03:55:04 [INFO] ~PandaHal

# Product Specifications

Pattern Controller Specification				
Processor	Application Processor	Dual-core ARM Cortex-A53		
	Real-time Processor	Dual-core ARM Cortex-R5		
Memory	Application Memory (DRAM)	2GB		
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	eMMC	8GB		
Peripheral	Ethernet	1G Ethernet		
	USB	USB2.0		
Debug	UART(USB)	USB to UART Bridge		
	JTAG	14pin/2.0mm		

Device Power Supply Specification						
Power Sources	Setting Range	Resolution	DC Accuracy	Max. Current		
VCC (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	1.2A		
VCCQ (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	400mA		
VPP (NAND)	5.0 to 20V	50mV	+/- (2% + 100mV)	80mA		
VREF (NAND)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA		
VCCIO (FPGA)	0.8 to 2.0V	1mV	+/- (1% + 20mV)	400mA		
VREFIO (FPGA)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA		

Pattern Generator Specification				
Command FIFO depth	64K			
Write Data Memory	64K Byte			
Read Data Memory	64K Byte			
Speed (SDR mode)	10 MHz			
Speed (DDR mode)	200 MHz ~ 800 MHz			
Resolution	< 1 MHz			
Output (CEn[7:0], ALE, CLE, WEn, REn, WPn)	22 pins * 2-channel			
Input (RBn[7:0])	8 pins * 2-channel			
I/O (DQS, DQ[7:0])	10 pins * 2-channel			
GPIO	8 pins			
	Command FIFO depth Write Data Memory Read Data Memory Speed (SDR mode) Speed (DDR mode) Resolution Output (CEn[7:0], ALE, CLE, WEn, REn, WPn) Input (RBn[7:0]) I/O (DQS, DQ[7:0])			

Environment Conditions	
<b>Operating Temperature</b>	0 ~ 70 °C
Humidity	20% ~ 60 Rh%
Dimensions & Weight	160 mm x 100 mm x 38mm ( W x L x H )
Power Supply	DC 12V / 2A
Host Interface	Ethernet

**trace L** test • verify + connect

