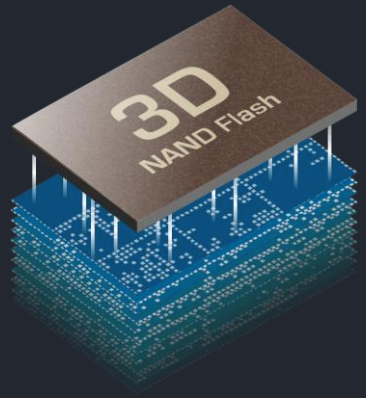
JTS250F HIGH-SPEED NAND TESTER

Product Brief

Access at anytime with our small, convenient and fast testing tools.



Sep.2019

Solution Brief

Connect

Connect Solution
- High-speed socket board
- Burn-in socket board
- Best signal quality and impedance matching
- Logic probing pad

Test

Test Solution
- Software-defined pattern
- Hardware-based timing
- Programmable Voltage & Frequency
- Embedded Linux and host programming environments

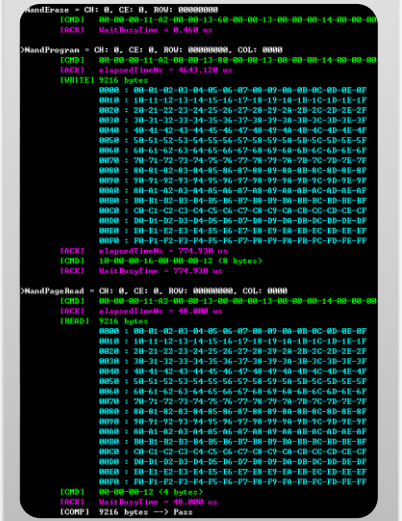
```
static void NandPageRead(byte ch, byte ce, int row, int col, ref byte[] data, int length)
{
    nand.SelectCE(ce);
    nand.Command(0xA2); // SLC mode transition
    nand.Command(0x00); // 1st set
    nand.AddressCol(col); // Address cycle
    nand.AddressRow(row); // Address cycle
    nand.CmdWithBusy(0x30, ce); // 2nd set: tR (70us / 80us)
    nand.ReadBytes(ref data, length); // Read Data
    nand.DeselectCE(ce);
}
```

Trace

Trace Solution
- Trace and debug with JKI NAND protocol analyzer
- Wave view
- List view
- Packet decoding

Verify

Analysis Solution
- NAND protocol analysis
- NAND cell analysis
- Power & Speed margin test
- User test APIs



Features & Advantages

Software-defined Pattern Generator

- Software-defined pattern generation logic provides very flexible and easy test programming environment for test engineer.

FPGA-based Timing Generator

- SDR mode: support legacy mode
- DDR mode: support source synchronous ddr mode clocking

Programmable Voltage & Frequency

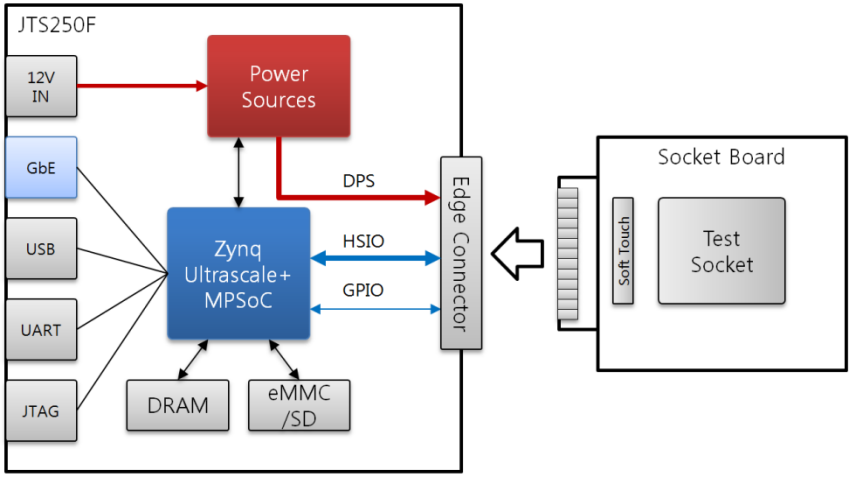
- Programmable power supplies
  (VCC, VCCQ, VPP, VCCIO, VREF, VREFIO)
- Programmable test speed up to 800 MHz

Best Signal Integrity

- Best signal integrity for high speed I/Os (HSIO)
- Additional general purpose I/Os (GPIO)

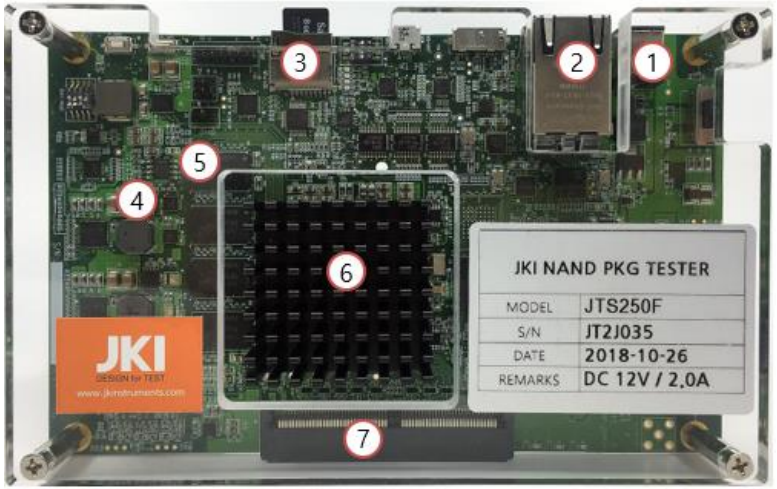
Applications

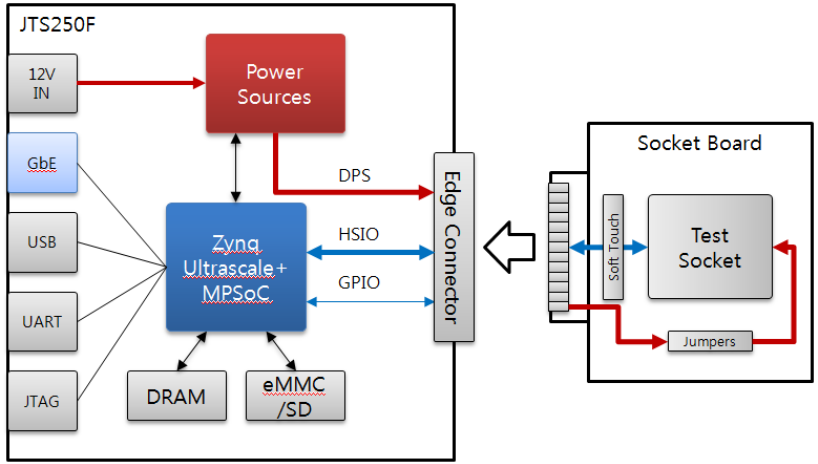
- Engineering test solution for high-speed DDR NAND devices



Test Board

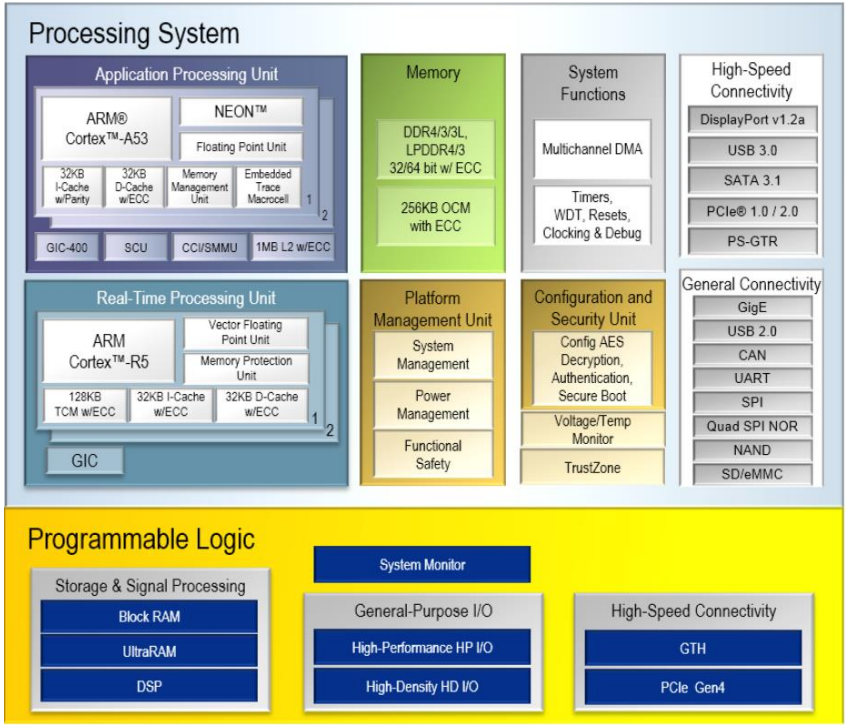
① Main Power Supply: 12V DC input
② Host Interface: Gigabit Ethernet
③ SD Card: Booting image and Firmware
④ Programmable Device Power Supplies
⑤ DRAM: Application Memory
⑥ Zynq (MPSoC + FPGA): Pattern Sequencer and Generator
⑦ Edge connector to connect Test board and Socket board



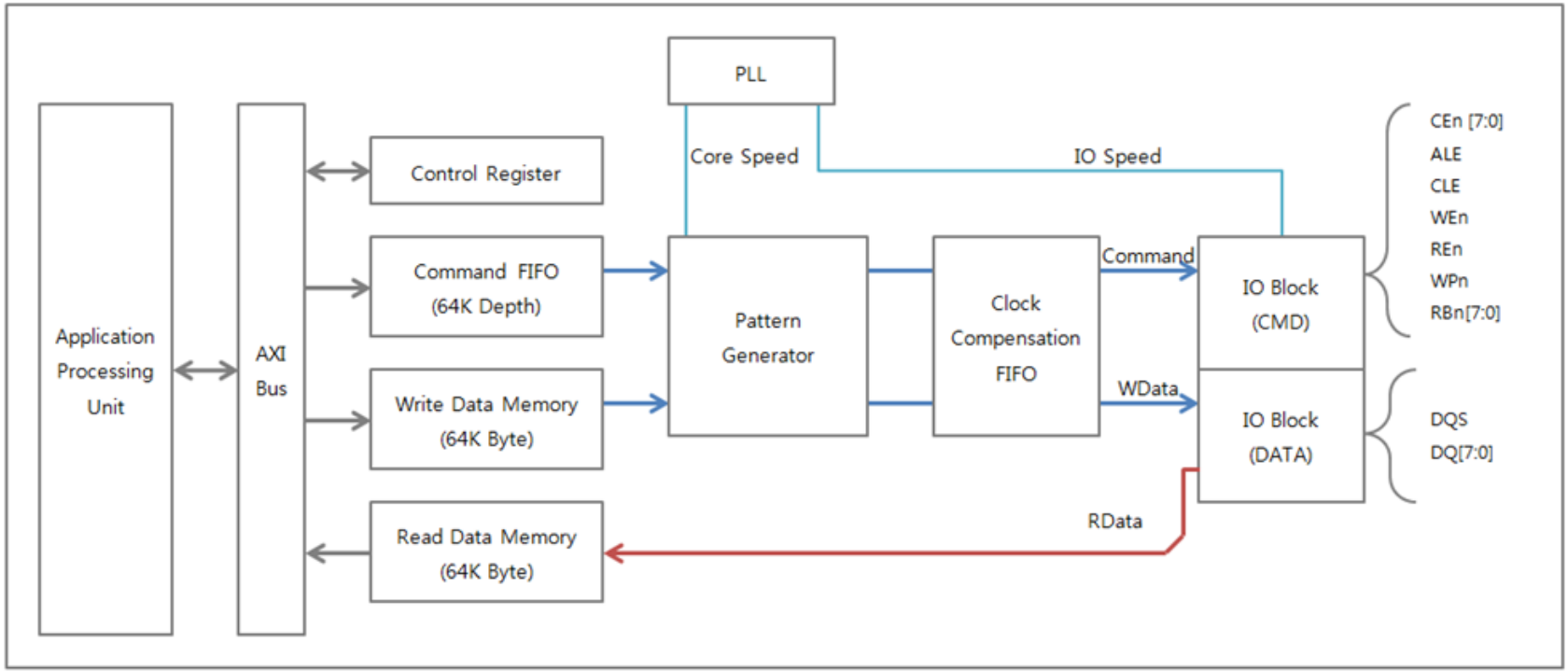


Pattern Controller

Pattern Controller Specification		
Processor	Application Processor	Dual-core ARM Cortex-A53
	Real-time Processor	Dual-core ARM Cortex-R5
Memory	Application Memory (DRAM)	2GB
	Micro-SD	8GB
	eMMC	8GB
Peripheral	Ethernet	1G Ethernet
	USB	USB2.0
Debug	UART(USB)	USB to UART Bridge
	JTAG	14pin/2.0mm



Pattern Generator



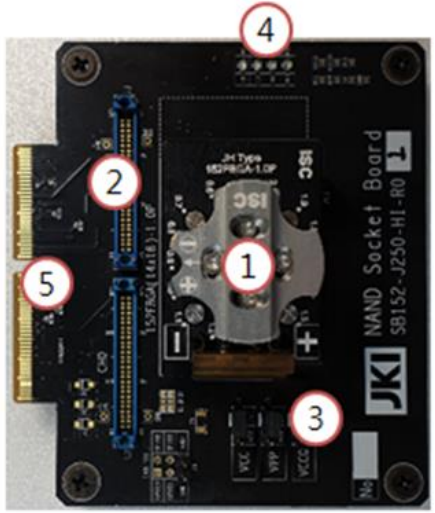
Device Power Supply

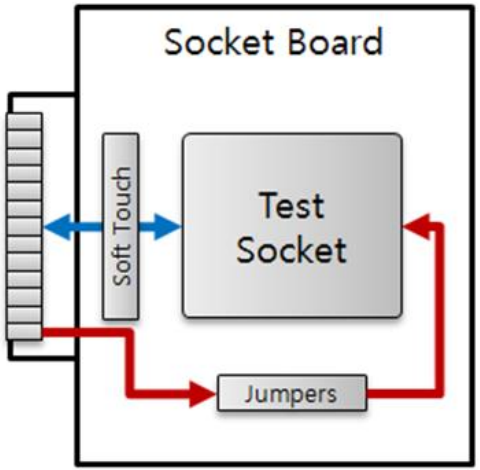
1. VCC: NAND device core power supply.
2. VCCQ: NAND I/O power supply.
3. VPP: NAND external high voltage.
4. VREF: NAND I/O reference voltage.
5. VCCIO: FPGA I/O power supply.
6. VREFIO: FPGA I/O reference voltage

Device Power Supply Specification				
Power Sources	**Setting Range**	**Resolution**	**DC Accuracy**	**Max. Current**
VCC (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	1.2A
VCCQ (NAND)	0.8 to 3.6V	1mV	+/- (1% + 20mV)	400mA
VPP (NAND)	5.0 to 20V	50mV	+/- (2% + 100mV)	80mA
VREF (NAND)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA
VCCIO (FPGA)	0.8 to 2.0V	1mV	+/- (1% + 20mV)	400mA
VREFIO (FPGA)	0.2 to 1.8V	1mV	+/- (1% + 20mV)	5mA

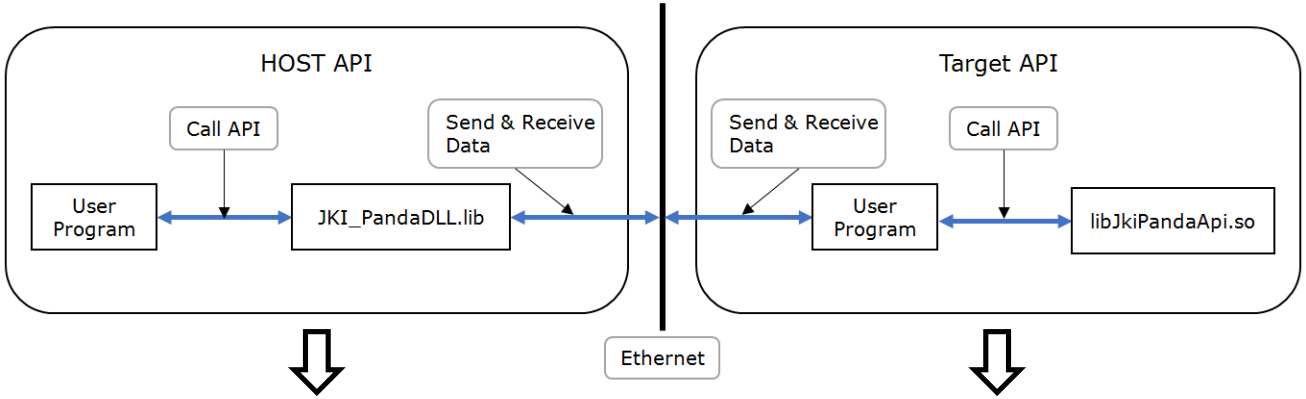
Socket Board

① Test Socket
② Logic analyzer probing pad
③ Power jumpers
④ LED indicators
⑤ Edge card

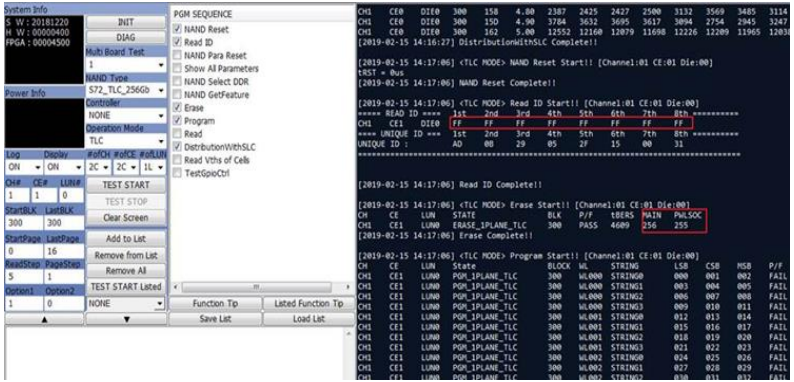




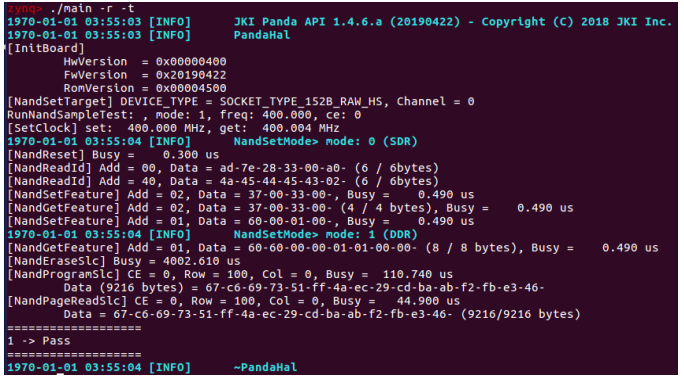
Software Architecture



Running on Remote PC (Host)



Running on Zynq Processor (Target)



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Pattern Generator Specification		
Pattern Generator	Command FIFO depth	64K
	Write Data Memory	64K Byte
	Read Data Memory	64K Byte
Clock Generator	Speed (SDR mode)	10 MHz
	Speed (DDR mode)	200 MHz ~ 800 MHz
	Resolution	< 1 MHz
Channels	Output (CEn[7:0], ALE, CLE, WEn, REn, WPn)	22 pins * 2-channel
	Input (RBn[7:0])	8 pins * 2-channel
	I/O (DQS, DQ[7:0])	10 pins * 2-channel
	GPIO	8 pins

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Environment Conditions	
Operating Temperature	0 ~ 70 ℃
Humidity	20% ~ 60 Rh%
Dimensions & Weight	160 mm x 100 mm x 38mm (W x L x H)
Power Supply	DC 12V / 2A
Host Interface	Ethernet

trace

test

verify

connect

JKI
DESIGN for TEST