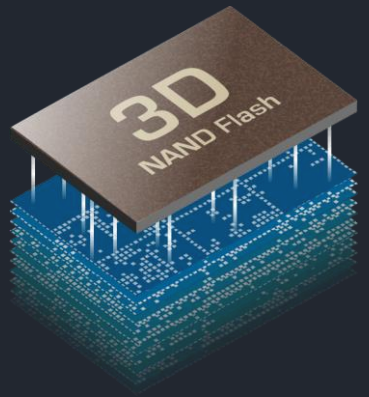
JKI NAND ENGINEERING TESTER (JTS350F/JTS351F)

Product Brief & Datasheet

Access at anytime with our small, convenient and fast testing tools.



June 2022

Solution Brief

Connect

High Speed Connecting

- High-speed DUT interface board & test sockets
- Best signal integrity
- Logic probing pads for logic debugging
- Power jumpers for current measurement

Test

High Speed Testing

- Software-defined pattern generator
- Hardware-based timing generator
- Programmable AC/DC parameters

Trace

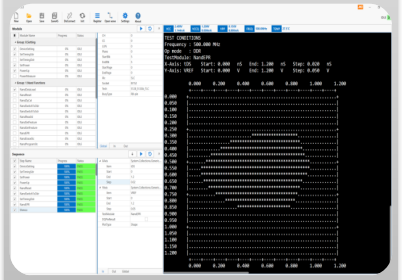
Tracing & Debugging

- Tracing and debugging with JKI NAND protocol analyzer
- Long-time lossless timing mode analysis
- Long-time lossless workload analysis by command filtering mode

Verify

Easy to Use

- Easy to develop test pattern program on embedded Linux
- Easy to use test sequence & parameter control on Windows
- Easy to debug by pattern simulation tool



Features & Advantages

Fast Control & Easy Development

- Fast MPSoC based test controller (ARM + FPGA)
- Easy test program development environment on Linux
- Easy sequence & parameter control environment on Windows

Software-defined Pattern Generator

- Software-defined command & data pattern generation
- Continuously streaming write and read data vector

Hardware-based Timing Generator

- Support 64 user defined timing sets
- Support source synchronous clocking

Programmable AC/DC Parameter

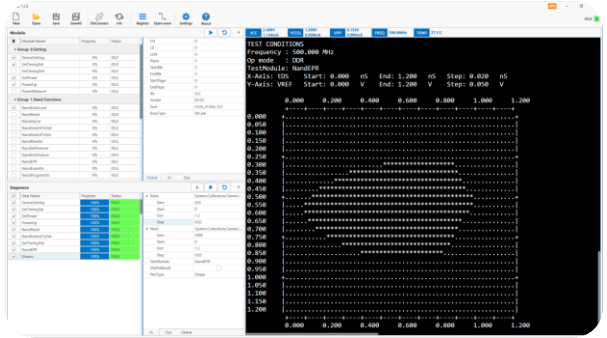
- Programmable power supplies (8 power sources)
- Programmable test speed up to 2400 Mbps (DDR)
- Programmable AC parameters

Best Signal Integrity

- Best signal integrity for high speed I/Os (HSIO)
- Additional general purpose I/Os (GPIO)

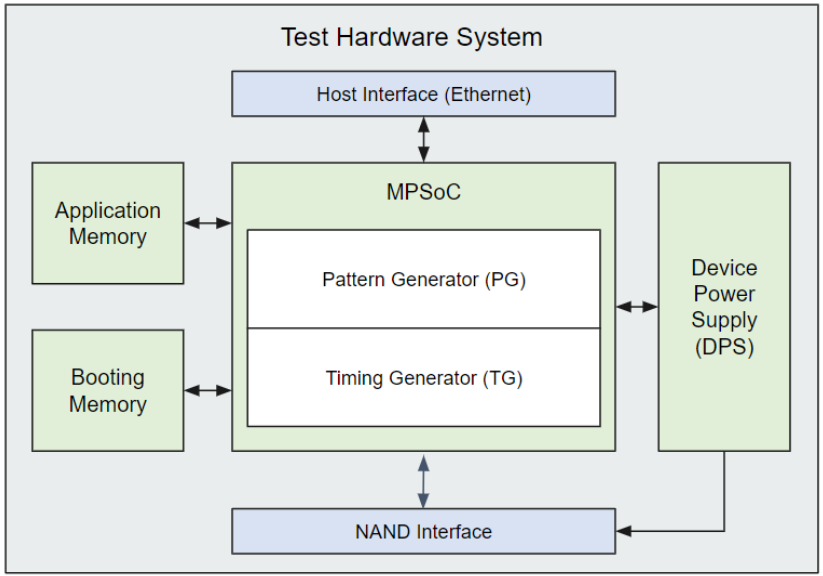
Applications

- Engineering test solution for high-speed DDR NAND devices



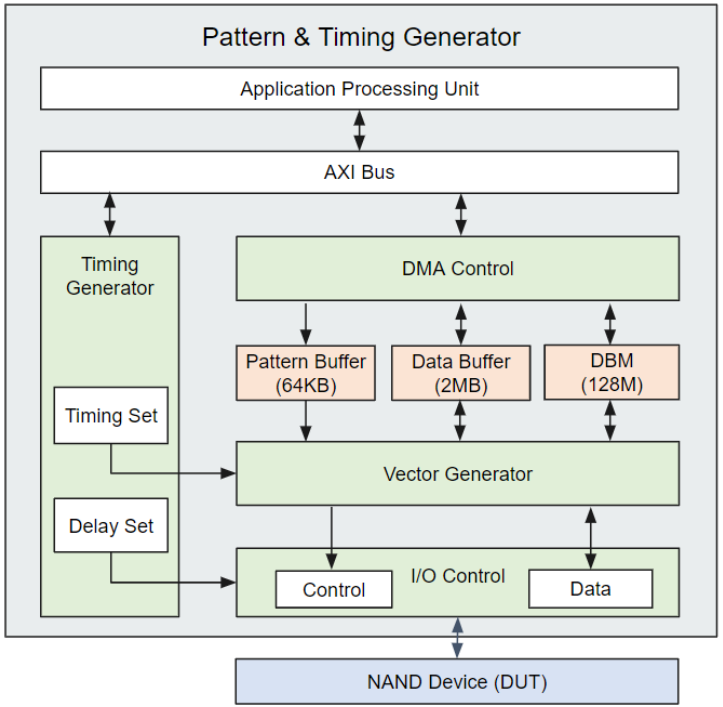
Hardware System Specifications

Hardware System Specifications		
Processor	Application Processor	Dual-core ARM Cortex-A53
	Real-time Processor	Dual-core ARM Cortex-R5
Memory	Application Memory	8GB (DDR4)
	Booting Memory	8GB (eMMC)
Host Interfaces	Ethernet	1G Ethernet
	USB	USB 2.0(Client), 3.0(OTG)
Debug Ports	UART	USB to UART Bridge
	JTAG	14 pin / 2.0 mm pitch
NAND Interfaces	HSIO	29 pin * 2 CH
	GPIO	8 pin
Device Power Supply	DPS for NAND	4 channels
	DPS for ETC	4 channels
Pattern & Timing Generator	PG	1 ea
	TG	1 ea



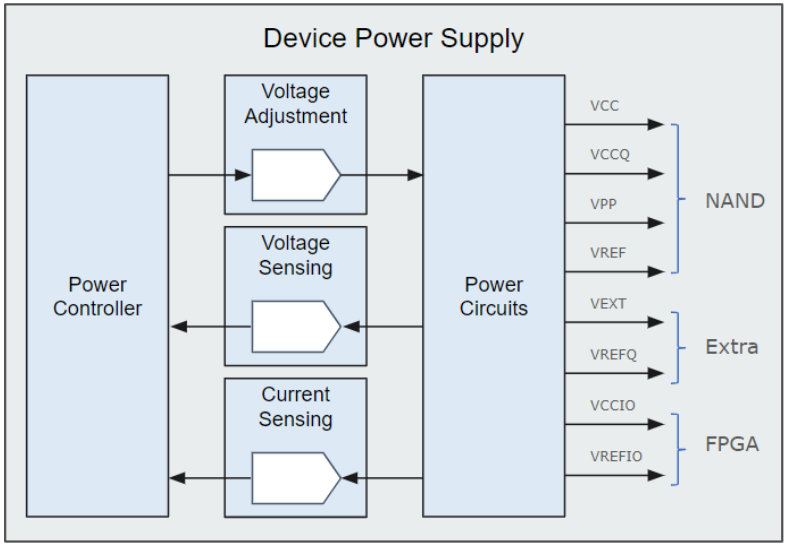
Pattern Generator Specifications

Pattern & Timing Generator Specifications		
Pattern Memory	Data Buffer Memory (DBM)	64MB(Write), 64MB(Read)
	Read/Write Data Buffer (FIFO)	2MB
	Pattern Buffer (FIFO)	64KB
Timing Generator	Clock Speed (SDR mode)	10 ~ 100 MHz
	Clock Speed (DDR mode)	100 MHz ~ 1200 MHz (200 Mb/s ~ 2400 Mb/s)
	Clock Resolution	1 MHz
	Timing Sets	64 ea
	Number of Edges for each Timing Set	64 ea
	Edge Control Range	1 ~ 256 UI
	Edge Control Resolution	1 UI (0.4 ~ 1.0 ns)
	Delay Control Range	0 ~ 1 ns
	Delay Control Resolution	3 ~ 4 ps
Pins	Output (CEn[7:0], Controls)	14 pins * 2-ch
	Input (RBn[3:0])	4 pins * 2-ch
	I/O (DQS, DQ[7:0], DBI)	11 pins * 2-ch
	GPIO	8 pins



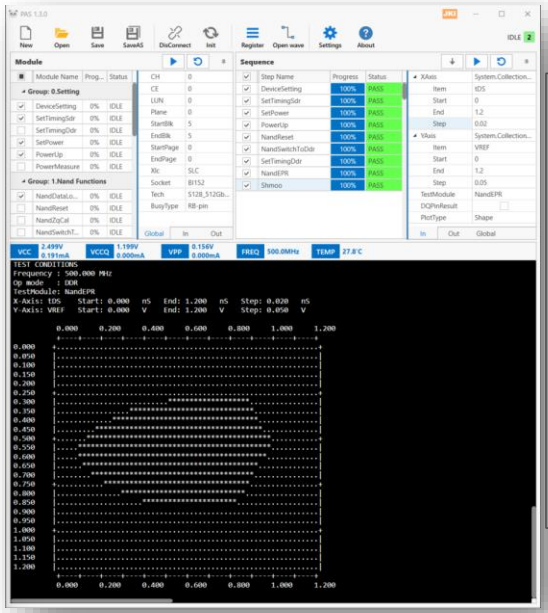
Power Supply Specifications

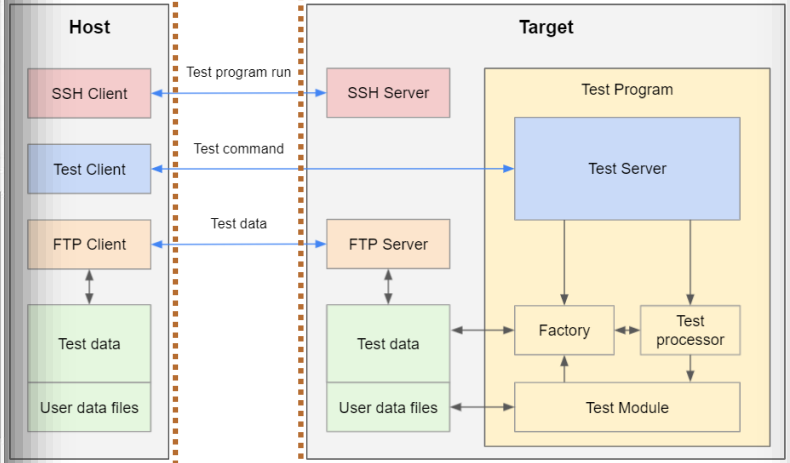
Device Power Supply Specifications				
Power Sources	**Setting Range**	**Resolution**	**DC Accuracy**	**Max. Current**
VCC (NAND)	0.8 to 3.6V	<1mV	+/- (1% + 2mV)	3A
VCCQ (NAND)	0.8 to 2.0V	<1mV	+/- (1% + 2mV)	400mA
VPP (NAND)	5.0 to 20V	<1mV	+/- (1% + 20mV)	80mA
VREF (NAND)	0.2 to 1.8V	<1mV	+/- (1% + 2mV)	10mA
VCCIO (FPGA)	0.8 to 2.0V	<1mV	+/- (1% + 2mV)	400mA
VREFIO (FPGA)	0.2 to 1.8V	<1mV	+/- (1% + 2mV)	10mA
VREFQ (Extra)	0.2 to 5.0V	<1mV	+/- (1% + 2mV)	15mA
VEXT (Extra)	1.2 to 30V	<1mV	+/- (1% + 20mV)	10mA



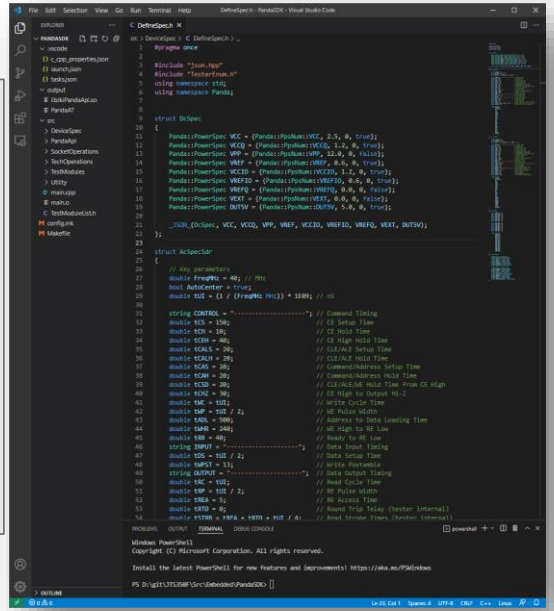
Software Architecture

Host Program
(Windows GUI based
Test Automation Studio)





Target Program
(Embedded Linux based
Test Pattern Programming)



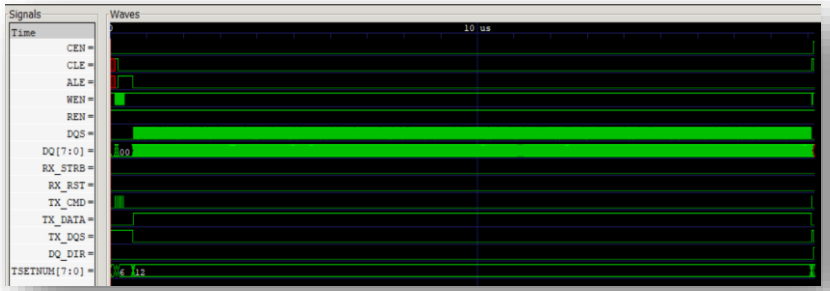
Pattern Programming & Verification

Test Pattern & Timing Sets

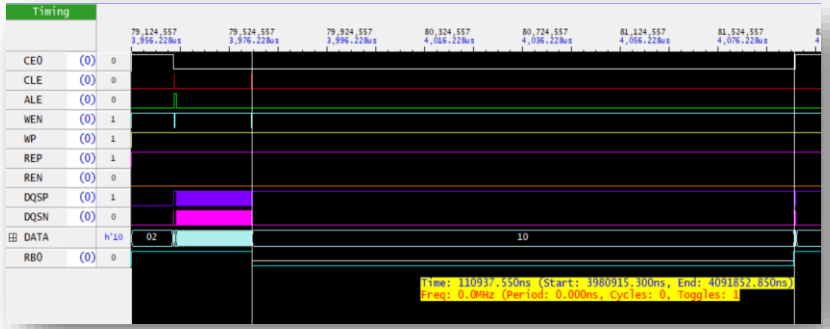
```
api->PG.Add(tset.Select);
api->PG.AddWriteData(tset.Command, 0xA2);
api->PG.AddWriteData(tset.Command, 0x80);
api->PG.AddWriteData(tset.Address, ColAddress_1st);
api->PG.AddWriteData(tset.Address, ColAddress_2nd);
api->PG.AddWriteData(tset.Address, RowAddress_1st);
api->PG.AddWriteData(tset.Address, RowAddress_2nd);
api->PG.AddWriteData(tset.Address, RowAddress_3rd);
api->PG.Add(tset.WrPre);
api->PG.AddWriteDBM(tset.WrDbm8B, 8, length / 8, DBM_Address);
api->PG.Add(tset.WrPostToCmd);
api->PG.AddWriteData(tset.Command, 0x10);
api->PG.AddBusy(tset.WaitReady);
api->PG.Add(tset.Deselect);
```

```
//-------------------------------------------------------
// Command latch cycle
//-------------------------------------------------------

double tS_max = std::max({tWP, tCALS, tCAS});
double tH_max = std::max({tCALH, tCAH});
rate = tS_max + tH_max;

api->TG.SetTime(tset.Command, PinNum::CEN, {{P, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::CLE, {{H, tS_max - tCALS}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::ALE, {{L, tS_max - tCALS}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::WEN, {{L, tS_max - tWP}, {H, tS_max}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::REN, {{H, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::WPN, {{H, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::RX_STRB, {{L, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::RX_RST, {{L, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::TX_CMD, {{L, 0}, {E, tS_max - tCAS}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::TX_DATA, {{L, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::TX_DQS, {{H, 0}, {P, rate}});
api->TG.SetTime(tset.Command, PinNum::DQ_DIR, {{L, 0}, {P, rate}});
```

Pattern Simulation



Logic Analyzer



Contact Us

Company	㈜제이케이아이 | JKI Inc.
CEO	JK Kang
Established	Jul, 2012
Business Area	Design and fabrication of test systems
Products and Services	**Trace Solutions** DDR3/4/5, LPDDR3/4/5, GDDR5/6 NAND, eMMC, MCP, etc. **Test Solutions** High-Speed Engineering Tester for DDR/NAND High-Speed Burn-In Tester for DDR/NAND **Connect Solutions** High-Speed Interposers for AP + Memory High-Speed Socket for DDR/NAND **Design Services** High-Speed Digital System Design High-Speed Test & Measurement Solution
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connect

test

trace

verify